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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WENDELL, ANDREW	
ART UNIT	PAPER NUMBER
2618	
MAIL DATE	DELIVERY MODE
07/09/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/813,327	SUH ET AL.	
	Examiner	Art Unit	
	ANDREW WENDELL	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *See Continuation Sheet* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,6-11,13,15,17-21,23,24,26,28-31,33,34,36,38-40,42,43,45,47 and 48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims pending in the application are 1,3,4,6-11,13,15,17-21,23,24,26,28-31,33,34,36,38-40,42,43,45,47 and 48.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3-4, 6-7, 9, 11, 15, 18-19, 21, 25-26, 29, 31, 33-36, 39-40, 42-43, and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Circello et al. (US Pat# 5,872,940) in view of Ryan (US Pat Pub# 2006/0277424) and further in view of Funk et al. (US Pat# 6,026,119).

Regarding claim 1, Circello teaches an application processor 101 (Fig. 1) having a central processing unit 102 (Fig. 1) and a first bus master controller 103 (Fig. 1) for controlling via a first common bus 107 (Fig. 1) a plurality of external peripherals 111, 112, and 113 (Fig. 1); and a shared memory (Col. 3 lines 38-40) connected to the AP 101 (Fig. 1) via the first common bus 107 (Fig. 1), wherein the first bus master controller 103 (fig. 1) controls the plurality of external peripherals by using a packet generator issuing a packetized command (Fig. 6 and 7, Col. 3 lines 10-12, it is obvious that the commands are packetized) commonly receivable by the plurality of external peripherals over the first common bus, and wherein the packetized command includes a module device select signal for selecting one of the plurality of external peripherals (Col. 3 lines 4-58). It is obvious that the shared memory of Circello can be connected to a modem from a second bus. However, Circello fails to teach a modulator/demodulator (modem)

connected to shared memory, a second bus master controller, and a digital signal processor.

Ryan teaches a shared memory 108 or 110 (Fig. 1) connected to the modem 104 (Fig. 1); an application processor 102 (Fig. 3) having a central processing unit 202 (Fig. 3) and a first bus master controller 211 or 214 (Fig. 3) for controlling via a first common bus 110 (Fig. 3) and a second bus master controller 246 or 250 (Fig. 3) for controlling via a second common bus 112 (Fig. 3), the shared memory 108 or 110 (Fig. 3) connected to the modem 104 (Fig. 3).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate a modulator/demodulator (modem) connected to shared memory as taught by Ryan into Circello's circuit in order to minimize power consumption and increasing the speed and functionality of the device (Section 0006).

Circello and Ryan fail to teach a digital signal processor.

Funk teaches a signal modulator/demodulator 101 (Fig. 4) having a digital signal processor for effecting radio communications (Col. 2 lines 44-53) and wherein the bus master controller 111 (fig. 4) controls the plurality of external peripherals by using a packet generator issuing a packetized command (Figs. 5-6) commonly receivable by the plurality of external peripherals over the first common bus, and wherein the packetized command includes a module device select signal for selecting one of the plurality of external peripherals (Col. 3 lines 26-45, Col. 4 line 45-Col. 5 line 26, and Fig. 5).

Therefore, it would have been obvious at the time of the invention to one of

ordinary skill in the art at the time the invention was made to incorporate a digital signal processor as taught by Funk into a modulator/demodulator (modem) connected to shared memory as taught by Ryan into Circello's circuit in order to reduce size, lower weight, and increase battery life (Col. 1lines 45-60).

Regarding claim 3, Circello further teaches a shared memory (SRAM, Col. 3 lines 38-40). It would have been obvious to use SDRAM as a possible choice for memory because of its size and performance.

Regarding claim 4, Circello further teaches wherein the plurality of external peripherals includes at least one of an image capture module and a display (Col. 3 lines 38-40).

Regarding claim 6, Funk et al. further teaches wherein the selected one of the plurality of external peripherals returns a signal to the bus master controller to acknowledge receipt (ARQ protocol) of the packetized command (Col. 7 lines 48-54).

Regarding claim 7, Circello further teaches wherein the packetized command includes a read/write command (Col. 3 line 38-Col. 4 line 34).

Regarding claim 9, Circello further teaches SRAM includes a plurality of data banks (Col. 3 line 38-Col. 4 line 34).

Ryan further teaches an interface for interfacing the second bus master controller 246 or 250 (Fig. 3) via the second common bus 112 (Fig. 3).

Regarding claim 11, Apparatus claim 11 is rejected for the same reason as apparatus claim 1 since the recited elements would perform the claimed steps.

Regarding claim 15, Funk et al. further teaches wherein the selected one of the plurality of peripherals returns a signal over the control lines of the first packet bus to the first master controller to acknowledge receipt (ARQ protocol) of the command (Col. 7 lines 48-54).

Regarding claim 18, Circello further teaches a shared memory (SRAM, Col. 3 lines 38-40). It would have been obvious to use SDRAM as a possible choice for memory because of its size and performance.

Regarding claim 19, Circello further teaches SRAM includes a plurality of data banks and an interface for interfacing (Col. 3 line 38-Col. 4 line 34).

Regarding claim 21, Circello teaches an application processor 101 (Fig. 1) comprising a central processing unit 102 (Fig. 1) for processing data received from a plurality of external peripherals and from a shared memory, a first bus master controller 103 (Fig. 1) for controlling via a first common bus 107 (Fig. 1) connected to the plurality of external peripherals 111, 112, and 113 (Fig. 1), and for interfacing with a shared memory (Col. 3 lines 4-58, it is obvious that the shared memory of Circello can be connected to a modem from a second bus), wherein the first bus master controller 103 (fig. 1) controls the plurality of external peripherals by using a packet generator issuing a packetized command commonly receivable by the plurality of external peripherals over the first common bus, and wherein the packetized command includes a module device select signal for selecting one of the plurality of external peripherals (Col. 3 lines 4-58). However, Circello fails to teach a modulator/demodulator (modem) connected to shared memory and a second bus master controller.

Ryan teaches a first bus master controller 211 or 214 (Fig. 3) for controlling via a first common bus 110 (Fig. 3); and a second bus master controller 246 or 250 (Fig. 3) for interfacing with the shared memory 108 or 110 (Fig. 3) via a second common bus 112 (Fig. 3), wherein the shared memory is connected to a signal modulator/demodulator (modem) 104 (Fig. 3).

Circello and Ryan fail to clearly teach packetized commands (even though it is obvious in Circello).

Funk teaches wherein the bus master controller 111 (fig. 4) controls the plurality of external peripherals by using a packet generator issuing a packetized command (Figs. 5-6) commonly receivable by the plurality of external peripherals over the first common bus, and wherein the packetized command includes a module device select signal for selecting one of the plurality of external peripherals (Col. 3 lines 26-45, Col. 4 line 45-Col. 5 line 26, and Fig. 5).

Regarding claim 23, the combination including Circello teaches a shared memory (SRAM, Col. 3 lines 38-40). It would have been obvious to use SDRAM as a possible choice for memory because of its size and performance.

Regarding claim 24, the combination including Circello teaches wherein the plurality of external peripherals includes at least one of an image capture module and a display (Col. 3 lines 38-40).

Regarding claim 26, Funk et al. further teaches wherein the selected one of the peripherals returns a signal to the first bus master controller to acknowledge receipt (ARQ protocol) of the packetized command packet (Col. 7 lines 48-54).

Regarding claim 29, the combination including Circello teaches SRAM includes a plurality of data banks (Col. 3 line 38-Col. 4 line 34)

Ryan further teaches an interface for interfacing the second bus master controller 246 or 250 (Fig. 3) via the second common bus 112 (Fig. 3).

Regarding claim 31, Apparatus claim 31 is rejected for the same reason as apparatus claim 21 since the recited elements would perform the claimed steps.

Regarding claim 33, the combination including Circello teaches a shared memory (SRAM, Col. 3 lines 38-40). It would have been obvious to use SDRAM as a possible choice for memory because of its size and performance.

Regarding claim 34, the combination including Circello teaches wherein the plurality of external peripherals includes at least one of an image capture module and a display (Col. 3 lines 38-40).

Regarding claim 36, Funk et al. further teaches wherein the selected one of the peripherals returns a signal to the bus master controller to acknowledge receipt (ARQ protocol) of the packetized command packet (Col. 7 lines 48-54).

Regarding claim 39, the combination including Circello teaches SRAM includes a plurality of data banks and an interface for interfacing the bus master controller via the first common bus (Col. 3 line 38-Col. 4 line 34).

Regarding claim 40, method claim 40 is rejected for the same reason as apparatus claims 21 and 31 since the recited elements would perform the claimed steps.

Regarding claim 43, the combination including Circello teaches wherein the plurality of external peripherals include at least one of an image capture module and a display (Col. 3 lines 38-40).

Regarding claim 45, Funk et al. further teaches wherein the selected one of the peripherals returns a signal to the first bus master controller to acknowledge receipt (ARQ protocol) of the packetized command packet (Col. 7 lines 48-54).

3. Claims 8, 17, 28, 38, and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Circello et al. (US Pat# 5,872,940) in view of Ryan (US Pat Pub# 2006/0277424) and further in view of Funk et al. (US Pat# 6,026,119) and further Watanabe et al. (US Pat# 6,378,102).

Regarding claim 8, Circello in view of Ryan and further in view of Funk teaches the limitations in claims 1 and 7. Circello, Ryan, and Funk fail to teach about a strobe signal.

Watanabe et al. synchronous semiconductor memory device with multi-bank configuration teaches wherein data read from the memory is sent out externally with a strobe signal, the strobe signal is for strobing the data read into a register in the master controller (Col. 1 line 64-Col. 2 line 10).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate a strobe signal

as taught by Watanabe et al. into a digital signal processor as taught by Funk into a modulator/demodulator (modem) connected to shared memory as taught by Ryan into Circello's circuit in order to have faster operation (Col. 2 lines 4-10).

Regarding claim 17, Watanabe et al. further teaches data read from the memory is transmitted out externally with a strobe signal, the strobe signal is used for strobing the data read into a register in the master controller (Col. 1 line 64-Col. 2 line 10).

Regarding claim 28, Watanabe further teaches wherein data read from the memory is sent out externally with a strobe signal, the strobe signal is for strobing the data read into a register in the master controller (Col. 1 line 64-Col. 2 line 10).

Regarding claim 38, Watanabe et al. further teaches wherein data read from the memory is sent out externally with a strobe signal, the strobe signal is for strobing the data read into a register in the master controller (Col. 1 line 64-Col. 2 line 10).

Regarding claim 47, Watanabe et al. further teaches wherein data read from the memory is sent out externally with a strobe signal, the strobe signal is for strobing the data read into a register in the master controller (Col. 1 line 64-Col. 2 line 10).

4. Claims 10 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Circello et al. (US Pat# 5,872,940) in view of Ryan (US Pat Pub# 2006/0277424) and further in view of Funk et al. (US Pat# 6,026,119) and further Fueki (US Pat Appl# 2002/0166058).

Regarding claim 10, Circello in view of Ryan and further in view of Funk teaches the limitations in claims 1 and 3. Circello, Ryan, and Funk fail to teach a protection signal.

Fueki's semiconductor integrated circuit on IC card protected against tampering teaches wherein the memory includes a first protection circuit and a second protection circuit for receiving address data from an external devices and for generating a protect signal upon receiving the same address from external devices (Sections 0014 and 0031).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate a protection signal as taught by Fueki into a digital signal processor as taught by Funk into a modulator/demodulator (modem) connected to shared memory as taught by Ryan into Circello's circuit in order to increase security (section 0015).

Regarding claim 20, Fueki further teaches wherein the memory includes a first protection circuit and a second protection circuit for receiving address data from an external devices and for generating a protect signal upon receiving the same address from external devices (Sections 0014 and 0031).

Regarding claim 30, Fueki further teaches wherein the memory includes a first protection circuit and a second protection circuit for receiving address data from an external devices and for generating a protect signal upon receiving the same address from external devices (Sections 0014 and 0031).

Regarding claim 48, Fueki further teaches wherein the memory includes a first protection circuit and a second protection circuit for receiving address data from an external devices and for generating a protect signal upon receiving the same address from external devices (Sections 0014 and 0031).

5. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Circello et al. (US Pat# 5,872,940) in view of Ryan (US Pat Pub# 2006/0277424) and further in view of Funk et al. (US Pat# 6,026,119) as applied to claim 11 above, and further in view of Wilska et al. (US Pat Appl# 2002/0082043).

Regarding claim 13, Circello in view of Ryan and further in view of Funk teaches the limitations in claim 11. Circello, Ryan, and Funk fail to teach an image capture module.

Wilska et al. device for personal communications teaches wherein the at least one peripheral is an image capture module 14 (Fig. 3).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate an image capture module as taught by Wilska et al. into a digital signal processor as taught by Funk into a modulator/demodulator (modem) connected to shared memory as taught by Ryan into Circello's circuit in order to collect data efficiently and to communicate with the environment (Section 0005).

Response to Arguments

Applicant's Remarks	Examiner's Response
"It is respectfully submitted that even	Ryan clearly teaches a second bus master

combining the selected portions of Circello, et al. with Ryan and Funk, et al., that a system as provided by the present invention involving an application processor that has first bus master controller communicating with external devices over a first common bus and a second bus master controller communicating with a shared memory that is connected to a modem over a second common bus is not disclosed or suggested in such combination of references. Clearly, Circello, et al. only provides a single system bus controller to which the system bus is connected."	controller 246 or 250 (Fig. 3). These controllers are direct memory access controllers which give direct control to the shared memories 108 and 110 (Fig. 3). Therefore, they can be considered a second bus master controller.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANDREW WENDELL whose telephone number is (571)272-0557. The examiner can normally be reached on 7:30-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nay Maung can be reached on 571-272-7882. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Andrew Wendell/
Examiner, Art Unit 2618

/Nay A. Maung/
Supervisory Patent Examiner, Art Unit 2618

6/30/2008